LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING
(AUTONOMOUS)
Accredited by NAAC with 'A' Grade, ISO 9001:2015 Certified Institution
Approved by AICTE, New Delhi and Affiliated to JNTUK, Kakinada
L.B.Reddy Nagar, Mylavaram-521230, Krishna Dist, Andhra Pradesh, India

DEPARTMENT OF ELECTRONIC AND COMMUNICATION ENGINEERING

REPORT ON EVENT ASIC / FPGA DESIGN & ITS APPLICATIONS

Event Type: Faculty Development Programme

Date / Duration: 22nd – 27th April, 2019.

Resource Persons: 1. Mr. B. Nagendra, Sr. Application Engineer, Apply Volt
2. Mr. J. Pradeep, Sr. Application Engineer, Apply Volt

Name of the Coordinator: Dr. P. Lachi Reddy, Professor

Audience: ECE, EEE and EIE Faculty

Total Number of Participants: 59

Objective of the Event: To train the faculty on advanced VLSI Design tools

Outcome of the Event: The participants are able to

1. Design various devices using full custom and semi custom design methods.
2. Design the testable devices.
3. Implement the design using Zed boards and ZYNQ boards.

Description / Report on Event:

Day one of the FDP started with the Inauguration Function, in which Principal, HOD, Co-ordinator and other dignitaries presented their views on the importance and objective of conducting the FDP and motivated all the participants to effectively utilize all the sessions and gain practical knowledge.

The resource persons from Apply Volt have given the presentation on "Basics of ASIC Design and ASICs Vs FPGAs". And have shown the Design flow of Full Custom and Semi Custom ASICs.

During day two, the resource person conducted hands on session on schematic design from Verilog/DFT Netlist, Adding Netlist to schematic Netlist, Adding Libraries, Extraction of schematic and analysis. In lab session, resource person given hands on experience on physical design, floor planning, placement & routing, Physical verification using industry standard caliber Tool.

Day three started with demonstration on Full custom design flow by resource persons with hands on experience covering Schematic entry, Spice models and simulation using the mentor graphics tools.

During day four, resource persons conducted the hands on training on Vivado tool. Design flow using Vivado tool and implementation of the design on Zed board and ZYNQ boards.

Day five and six, completely for lab sessions on the tools learned during previous four days.

Feedback / Suggestions:

1. Good hospitality
2. More number of workshops/FDPs on similar advanced tools

Photographs:

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Addressing by Resource person</td>
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Day 1: Lab session</td>
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Day 2: Lab session</td>
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Day 4: Lab session</td>
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Day 6: Lab session</td>
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Certificate Presentation to Participant</td>
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